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[57] ABSTRACT

The entire data path of a synchronous integrated circuit device is initialized in a test mode upon power-up of the synchronous integrated circuit device. Upon power-up of the integrated circuit device in the test mode, a clock signal (either an external clock signal or an associated internal clock signal) is internally clocked. As the clock signal goes to a low logic state upon power-up of the device, a master latch (flip-flop) element of the integrated circuit device is loaded with data and is allowed to conduct; a slave latch (flip-flop) element of the integrated circuit device does not conduct. As the clock signal goes to a high logic state, the data in the master latch is latched. Also upon the high logic state of the clock the slave latch element is loaded with data and is allowed to conduct.

17 Claims, 4 Drawing Sheets